In the Claims

Claims 1-2 are canceled.

3. [Currently Amended] A method of forming a conductive capacitor plug in a ~~capacitor-over-bit line~~ memory array, the method comprising extending conductive material from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line, wherein the extending comprises etching a contact opening through insulative material after forming said bit line and forming conductive material within the contact opening, wherein the forming of the conductive material comprises forming a storage capacitor at least partially within the contact opening.

4. [Previously Presented] The method of claim 3, wherein the extending comprises etching a contact opening through two separately-formed insulative material layers, at least a portion of the contact opening being generally self-aligned to said bit line, and forming conductive material within the contact opening.

5. [Previously Presented] The method of claim 3, wherein the array comprises a word line elevationally below the bit line, and the extending comprises etching a contact opening through insulative material and generally self-aligned to both said bit line and said word line.

6. [Original] The method of claim 5, wherein the insulative material comprises two or more separately-formed insulative material layers.

7. [Previously Presented] The method of claim 3, wherein the extending comprises:

forming a patterned masking layer over the substrate and defining an opening pattern over said substrate node location;

etching insulative material through the opening pattern sufficient to form a contact opening after forming said bit line; and

forming conductive material within the contact opening.

8. [Original] The method of claim 7, wherein said opening pattern is formed over a plurality of substrate node locations over which individual capacitors are to be formed.

9. [Previously Presented] The method of claim 3, wherein said substrate node location comprises a diffusion region, and the extending comprises:

etching a contact opening through insulative material to substantially expose a portion of the diffusion region after forming said bit line; and

forming conductive material within the contact opening and in electrical communication with the diffusion region.

10. [Original] The method of claim 9, wherein said insulative material comprises two separately-formed layers of insulative material.

11. [Previously Presented] A method of forming a capacitor contact opening in a capacitor-over-bit line memory array, the method comprising etching an opening through a first insulative material received over a bit line and a word line substantially selective relative to second insulative material covering the bit line and the word line to a substrate location proximate the word line in a self-aligning manner relative to both the bit line and the word line.

12. [Original] The method of claim 11, wherein the first insulative material comprises separately-formed layers of insulative material.

13. [Original] The method of claim 11, wherein the first insulative material comprises two separately-formed layers of insulative material.

14. [Original] The method of claim 11, wherein the second insulative material separately encapsulates the bit line and the word line.

15. [Original] The method of claim 11, wherein the substrate location comprises a diffusion region, and the etching comprises outwardly exposing the diffusion region.

16. [Original] The method of claim 11, wherein the etching comprises removing all of the first insulative material from over the bit line.

17. [Original] The method of claim 11, wherein the etching comprises forming a patterned masking layer over the first insulative material defining an opening pattern, and etching the opening through the opening pattern.

18. [Original] The method of claim 11, further comprising forming conductive material within the opening, the conductive material extending to an elevation laterally proximate conductive portions of the bit line.

19. [Original] The method of claim 11 further comprising forming conductive material within the opening, the conductive material extending to a location elevationally higher than any conductive portion of the bit line.

20. Canceled.

21. [Previously Presented] The method of claim 24, wherein the etching comprises etching openings down to proximate individual substrate diffusion regions.

22. [Previously Presented] The method of claim 24, wherein the etching comprises etching openings down to proximate individual word lines of the array.

23. [Original] The method of claim 22, wherein the etching comprises exposing individual substrate diffusion regions intermediate the word lines.

24. [Previously Presented] Etching an array of capacitor contact openings in a capacitor-over-bit line memory array to elevationally below the bit lines after forming the bit lines, wherein etching comprises selectively etching through first insulative material relative to second insulative material covering portions of the bit lines.

25. [Previously Presented] Etching an array of capacitor contact openings in a capacitor-over-bit line memory array to elevationally below the bit lines after forming the bit lines, wherein the etching comprises selectively etching through first insulative material relative to second insulative material covering portions of the bit lines and word lines of the array.

26. [Previously Presented] A method as claimed in claim 25, wherein the first insulative material comprises a plurality of separately formed layers of first insulative material.

27. [Previously Presented] A method as claimed in claim 24, further comprising forming conductive material within the contact openings, the conductive material extending to at least laterally proximate conductive portions of the bit lines.

28. [Previously Presented] A method as claimed in claim 24, further comprising forming conductive material within the contact openings, the conductive material extending elevationally higher than any conductive portions of the bit lines.

29. [Original] A method of forming a capacitor-over-bit line memory array comprising:

forming a plurality of word lines over a substrate, the word lines having insulating material thereover;

forming a plurality of bit lines over the word lines, the bit lines having insulating material thereover;

forming insulative material over the word lines and the bit lines, the insulative material being etchably different from the insulating material over the word lines and the insulating material over the bit lines; and

selectively etching capacitor contact openings through the insulative material relative to the insulating material over the bit lines and the insulating material over the word lines, the openings being self-aligned to both bit lines and word lines and extending to proximate the substrate.

30. [Original] The method of claim 29, wherein the forming of the insulative material comprises forming a plurality of layers of insulative over at least one of the word lines and bit lines.

31. [Original] The method of claim 29, wherein forming of the insulative material comprises forming one layer of insulative material over the word lines, and after the forming of the bit lines, forming another layer of insulative material over the bit lines.

32. [Original] The method of claim 31, further comprising forming a patterned masking layer over the insulative material defining a mask opening, the mask opening being received over a plurality of substrate locations over which the capacitor contact openings are to be etched, and the etching of the capacitor contact openings comprises etching said contact openings through said mask opening.

33. [Original] The method of claim 29, further comprising forming conductive material within the contact openings, the conductive material being formed to extend from proximate individual substrate diffusion regions to at least locations which are elevationally coincident with conductive material of the individual bit lines.

34. [Original] The method of claim 29, further comprising forming conductive material within the contact openings, the conductive material being formed to extend from proximate individual substrate diffusion regions to locations elevationally higher than any conductive material of any of the bit lines.

35. Canceled.

36. [Previously Presented] A method of forming a capacitor-over-bit line memory array comprising:

forming a plurality of word lines over a substrate;

forming a plurality of bit lines over the word lines;

forming insulative material over the word lines and the bit lines; and

after forming the bit lines, etching an opening through the insulative material and outwardly exposing a diffusion region received within the substrate proximate a word line, wherein the forming of the insulative material comprises forming two separate layers of insulative material over the substrate, and the etching of the opening comprises etching the two layers selectively relative to insulative coverings formed over portions of both the bit lines and the word lines.

37. [Previously Presented] The method of claim 36, further comprising forming conductive material within the opening, the conductive material extending from proximate the diffusion region to a location elevationally higher than any conductive material of the bit lines.

38. Canceled.

39. [Previously Presented] The method of claim 43, wherein the memory array is a capacitor-over-bit line memory array.

40. [Previously Presented] The method of claim 43, wherein the bit line plug and bit line comprise at least one common material.

41. [Previously Presented] The method of claim 43, wherein the bit line plug and bit line comprise at least one common material, said common material being deposited in a common processing step.

42. [Previously Presented] The method of claim 43, wherein the forming of the capacitor plug comprises forming said surface elevationally higher than any conductive portion of the bit line.

43. [Previously Presented] A method of forming a memory array comprising in sequence:

forming a plurality of conductive lines over a substrate;

forming a conductive bit line plug intermediate a pair of the conductive lines;

forming a bit line in electrical communication with the conductive bit line plug;

forming a conductive capacitor plug proximate one of the pair of conductive lines, which capacitor plug extends away from the substrate and terminates above conductive portions of the bit line; and

forming a capacitor over and in electrical communication with the capacitor plug, and further comprising, prior to the forming of the conductive bit line plug, forming first insulative material over the conductive lines, and wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the conductive lines.

44. [Previously Presented] A method of forming a memory array comprising in sequence:

forming a plurality of conductive lines over a substrate;

forming a conductive bit line plug intermediate a pair of the conductive

lines;

forming a bit line in electrical communication with the conductive bit line plug;

forming a conductive capacitor plug proximate one of the pair of conductive lines, which capacitor plug extends away from the substrate and terminates above conductive portions of the bit line; and

forming a capacitor over and in electrical communication with the capacitor plug, and further comprising, prior to the forming of the conductive capacitor plug, forming first insulative material over the bit line, and wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the bit line.

45. [Previously Presented] A method of forming a memory array comprising in sequence:

forming a plurality of conductive lines over a substrate;

forming a conductive bit line plug intermediate a pair of the conductive lines;

forming a bit line in electrical communication with the conductive bit line plug;

forming a conductive capacitor plug proximate one of the pair of conductive

lines, which capacitor plug extends away from the substrate and terminates above conductive portions of the bit line; and

forming a capacitor over and in electrical communication with the capacitor plug, and further comprising:

prior to the forming of the conductive bit line plug, forming a first layer of first insulative material over the conductive lines; and

prior to the forming of the conductive capacitor plug, forming a second layer of first insulative material over the bit line,

wherein the forming of the conductive capacitor plug comprises substantially selectively etching an opening into the first insulative material relative to second insulative material over the conductive lines and bit line.

46. [Original] The method of claim 45, wherein the etching comprises exposing a substrate diffusion region proximate the conductive lines.

47. Canceled.

48. [Original] A method of forming a memory array comprising:

forming a plurality of word lines over a substrate, the word lines having insulating material thereover;

forming a plurality of bit lines over the word lines, the bit lines having

insulating material thereover;

forming insulative material over the word lines and the bit lines, the insulative material being etchably different from the insulating material over the word lines and the insulating material over the bit lines; and

selectively etching contact openings through the insulative material relative to the insulating material over the bit lines and the insulating material over the word lines, the openings being self-aligned to both bit lines and word lines and extending to proximate the substrate.

49. [Currently Amended] A method of forming a conductive capacitor plug in a ~~capacitor-over-bit line~~ memory array employing shallow trench isolation, the method comprising extending conductive material from proximate a substrate node location to a location elevationally above all conductive material of an adjacent bit line; and

wherein the array comprises a word line elevationally below the bit line, and the extending comprises etching a contact opening through insulative material and generally self-aligned to both said bit line and said word line.

50. [Previously Presented] The method of claim 49, wherein the extending comprises etching a contact opening through insulative material after forming said bit line and forming conductive material within the contact opening.

51. [Previously Presented] The method of claim 50, wherein the forming of the conductive material comprises forming a storage capacitor at least partially within the contact opening.

52. [Previously Presented] The method of claim 49, wherein the extending comprises etching a contact opening through two separately-formed insulative material layers, at least a portion of the contact opening being generally self-aligned to said bit line, and forming conductive material within the contact opening.

53. [Previously Presented] The method of claim 49, wherein the insulative material comprises two or more separately-formed insulative material layers.

54. [Previously Presented] The method of claim 49, wherein the extending comprises:

forming a patterned masking layer over the substrate and defining an opening pattern over said substrate node location;

etching insulative material through the opening pattern sufficient to form a contact opening after forming the bit line; and

forming conductive material within the contact opening.

55. [Previously Presented] The method of claim 54, wherein the opening pattern is formed over a plurality of substrate node locations over which individual capacitors are to be formed.

56. [Previously Presented] The method of claim 49, wherein the substrate node location comprises a diffusion region, and the extending comprises:

etching a contact opening through insulative material to substantially expose a portion of the diffusion region after forming the bit line; and

forming conductive material within the contact opening and in electrical communication with the diffusion region.

57. [Previously Presented] The method of claim 56, wherein the insulative material comprises two separately-formed layers of insulative material.

58. [Previously Presented] The method of claim 3, wherein the forming the storage capacitor at least partially within the contact opening comprises forming electrically conductive and electrically insulative material of the storage capacitor within the contact opening.

59. [Previously Presented] A method as claimed in claim 24, wherein the etching through the first insulative material relative to the second insulative material comprises leaving the second insulative material substantially unetched during and after the etching.

60. [Previously Presented] A method as claimed in claim 24 wherein the first insulative material and the second insulative material individually comprise a layer having a surface substantially parallel to a surface of a substrate of the memory array.

61. [Previously Presented] A method as claimed in claim 25, wherein the etching through the first insulative material relative to the second insulative material comprises leaving the second insulative material substantially unetched during and after the etching.

62. [Previously Presented] The method of claim 36, wherein the insulative coverings contact respective ones of the portions of the bit lines and the word lines.

63. [New] The method of claim 3 wherein the forming the conductive material comprises forming a first electrode of the storage capacitor, and further comprising forming a dielectric layer of the storage capacitor within the contact opening and configured to insulate the first electrode from a second electrode of the storage capacitor.

64. [New] The method of claim 63 further comprising forming at least a portion of the second electrode within the contact opening.

65. [New] The method of claim 49 wherein the extending the conductive material comprises forming a first electrode of the storage capacitor, and further comprising forming a dielectric layer of the storage capacitor within the contact opening and configured to insulate the first electrode from a second electrode of the storage capacitor.

66. [New] The method of claim 65 further comprising forming at least a portion of the second electrode within the contact opening.